What is claimed is:

1. A method for forming a well, the method comprising:

forming an isolation trench in a semiconductor substrate;

selectively performing low-energy, high-dose ion implantation through the bottom of the trench, thereby forming a high-concentration well therebeneath;

filling the trench with an insulating layer, thereby forming an isolation layer in the high-concentration well; and

performing low-energy, low-dose ion implantation on the semiconductor substrate including the isolation layer, thereby forming a low-concentration well in the semiconductor substrate to a depth partially overlapping with an upper portion of the high-concentration well.

2. The method of claim 1, wherein the isolation trench has a depth of about 2500 to about 3000 Å.

3. The method of claim 1, wherein the low-energy, high-dose ion implantation is performed at an energy level about 10 to about 30 keV and at a dose of about 1×10^{15} to about 5×10^{15} ions/cm^2.

4. The method of claim 1, wherein the low-energy, low-dose ion implantation is performed with impurities at an energy level about 20 to about 30 keV and at a dose of about 1×10^{12} to about 1×10^{13} ions/cm^2

5. The method of claim 1, wherein the low-concentration well is formed to the bottom of the trench.

6. The method of claim 1, wherein the total depth of the low-concentration well and the high-concentration well is about the same as the depth of the isolation layer.

7. A method for forming a well, the method comprising:

forming a pad nitride layer pattern on a semiconductor substrate;

etching the semiconductor substrate, using the pad nitride layer pattern as an etch mask, thereby forming an isolation trench in the semiconductor substrate;

forming a spacer nitride layer on inner walls of the trench;

selectively performing low-energy, high-dose ion implantation, using the pad nitride layer pattern and the spacer nitride layer as an ion implantation mask, thereby forming a high-concentration well therebeneath;

filling the trench with an insulating material, thereby covering the high-concentration well;

planarizing the insulating material to form an insulating layer in the trench, and removing the pad nitride layer pattern; and

performing low-energy, low-dose ion implantation on the semiconductor substrate including the isolation layer, thereby forming a low-concentration well in the semiconductor substrate to a depth partially overlapping with an upper portion of the high-concentration well.

8. The method of claim 7, wherein the isolation trench has a depth of about 2500 to about 3000 Å.

9. The method of claim 7, wherein for the low-energy, high-dose ion implantation is performed with impurities at an energy level about 10 to about 30 keV and at a dose of about 1×10^{15} to about 5×10^{15} ions/cm^2.

10. The method of claim 7, wherein the low-energy, low-dose ion implantation is performed with impurities at an energy level 20 to 30 keV and at a dose of 1×10^{12} to 1×10^{13} ions/cm2.

11. The method of claim 7, before forming the spacer nitride layer on the inner walls of the trench, further comprising forming a liner oxide layer on the inner walls and on bottom of the trench.

12. A method for forming a well, the method comprising:

forming a pad nitride layer pattern on a semiconductor substrate having first and second regions;

etching the semiconductor substrate, using the pad nitride layer pattern as an etch mask, thereby forming isolation trenches in the first and second regions;

forming a spacer nitride layer on inner walls of the trenches;

forming a first photoresist pattern on the resulting structure to expose only the second region and performing low-energy, high-dose ion implantation, using the pad nitride layer pattern and the spacer nitride layer as an ion implantation mask, thereby forming a high-concentration well of a first conductivity type at the bottom of the trench in the second region;

removing the first photoresist pattern, forming a second photoresist pattern for exposing only the first region, and performing low-energy, high-dose ion implantation, using the pad nitride layer pattern and the spacer nitride layer as an ion implantation mask, thereby forming a high-concentration well of a second conductivity type, which is different from the first conductivity type, at the bottom of the trench in the first region;

removing the second photoresist pattern, covering the high-concentration well of the first conductivity type and the high-concentration well of the second conductivity type with an insulating material, planarizing the top surface of the insulating material, and removing the pad nitride layer pattern, thereby forming an isolation layer to fill the trenches;

forming a third photoresist pattern for exposing only the second region, and performing low-energy, low-dose ion implantation on the semiconductor substrate including the isolation layer, thereby forming a low-concentration well of the first conductivity type in the second region to a depth partially overlapping with an upper portion of the high-concentration well of the first conductivity type;

removing the third photoresist pattern, forming a fourth photoresist pattern for exposing only the first region, and performing low-energy, low-dose ion implantation on the semiconductor substrate including the isolation layer; and removing the fourth photoresist pattern, thereby forming a low-concentration well of the second conductivity type in the first region to a depth partially overlapping with an upper portion of the high-concentration well of the second conductivity type.

13. The method of claim 12, wherein the isolation trench has a depth of 2500 to 3000 Å.

14. The method of claim 12, wherein the low-energy, high-dose ion implantation is performed with impurities at an energy level about 10 to about 30 keV and at a dose of about 1×10^{15} to about 5×10^{15} ions/cm^2.

15. The method of claim 12, wherein the low-energy, low-dose ion implantation is performed with impurities at an energy level about 20 to about 30 keV and at a dose of about 1×10^{12} to about 1×10^{13} ions/cm^2

16. The method of claim 12, before forming the spacer nitride layer on the inner walls of the trenches, further comprising forming a liner oxide layer on the inner walls and on bottoms of the trenches.

17. The method of claim 12, wherein the first through fourth photoresist patterns are formed to a thickness of about 1 to about 1.5 μm to obtain a sufficient margin between adjacent wells.

18. A method for forming a well, the method comprising:

forming an isolation trench in a semiconductor substrate;

performing a first ion implantation process at a first energy level and at a first dose through the bottom of the trench, thereby forming a high-concentration well therebeneath;

filling the trench with an insulating material, thereby forming an isolation layer in the high-concentration well; and

performing a second ion implantation process at a second energy level higher than the first energy level and at a second dose lower than the first dose on the semiconductor substrate including the isolation layer, thereby forming a low-concentration well in the semiconductor substrate to substantially the bottom of the trench.

19. The method of claim18, wherein the first energy level is about 10 to about 30 keV and the first dose is about 1×10^{15} to about 5×10^{15} ions/cm^2.

20. The method of claim 18, wherein the second energy level is about 20 to about 30 keV and the second dose is about 1×10^{12} to about 1×10^{13} ions/cm^2.